RGC Ref.: N_HKUST636/13 NSFC Ref. : 61361166007
(please insert ref. above)

The Research Grants Council of Hong Kong
NSFC/RGC Joint Research Scheme
Joint Completion Report

(Please attach a copy of the completion report submitted to the NSFC by the Mainland researcher)

Part A: The Project and Investigator(s)

1. Project Title

Investigation of the bulk and interface traps in III-nitride semiconductor heterostructure power electronic devices

2. Investigator(s) and Academic Department/Units Involved

	Hong Kong Team	Mainland Team
Name of Principal Investigator *(with title)*	Prof. Jing Kevin Chen (陳敬教授)	Prof. Bo Shen (沈波教授)
Post	Professor （教授）	Professor （教授）
Unit / Department / Institution	Department of Electronic and Computer Engineering, HKUST 香港科技大學電子及計算機工程系	School of Physics, Peking University 北京大學物理學院
Contact Information	Email: eekjchen@ust.hk Tel: 852-23588969	Email: bshen@pku.edu.cn Tel: 010-62767809
Co-investigator(s) *(with title and institution)*	Prof. Jiannong Wang (王建農教授) Department of Physics, HKUST 香港科技大學物理系	Dr. Maojun Wang (王茂俊Lecturer) Institute of Microelectronics, Peking Univ. 北京大學微電子所 Dr. Fujun Xu (許福軍Lecturer) School of Physics, Peking Univ. 北京大學物理學院 Dr. XuelinYang (楊學林engineer) School of Physics, Peking Univ. 北京大學物理學院

3. Project Duration

	Original	Revised	Date of RGC/ Institution Approval *(must be quoted)*
Project Start date	2014-01-01		
Project Completion date	2017-12-31		
Duration *(in month)*	48		
Deadline for Submission of Completion Report	2018-12-31		

Part B: The Completion Report

5. Project Objectives

5.1 Objectives as per original application

1. Develop temperature- and time-dependent high-field characterization techniques for studying bulk traps in III-nitride material systems
2. Develop temperature- and time-dependent characterization techniques for studying interface traps in III-nitride MIS-HEMT structures
3. Develop optimized structures and growth techniques of the buffer layer for III-nitride lateral power electronic devices

4. Evaluate various dielectric materials in III-nitride MIS-HEMTs and determine optimized dielectric technology

5.2 Revised Objectives

Date of approval from the RGC: ____________________

Reasons for the change: ____
____

6. Research Outcome

Major findings and research outcome

(maximum 1 page; please make reference to Part C where necessary)

With our effort in this project period, achievements have been made in characterizing the interface/bulk traps, understanding the underlying physical mechanisms and addressing the trap-related issues. Effective temperature- and time-dependent characterization techniques have been developed for studying the bulk/interface traps in III-nitride material systems. With the developed characterization methods, the physical mechanisms of trap-related issues have been investigated in-depth. These studies provide substantial guidelines for the optimization of the III-nitride power electronic devices.

Through improvement of device structure and fabrication process, bulk/interface traps-induced issues, including current collapse and V_{TH} instability, have been addressed with approaches that can be practically implemented. Bulk-trap induced current collapse has been effectively suppressed by seamlessly on-chip integration of the Schottky-on-heterojunction light-emitting diode (SoH-LED) or photonic-ohmic drain with the AlGaN/GaN HEMT. High-quality dielectric/III-nitride interface has been obtained using nitridation treatment and interface protection techniques. With these techniques, highly reliable LPCVD-SiN_x has been successfully applied in the MIS-FETs with fully-recessed gate structure to achieve high-performance E-mode device with long TDDB-lifetime of gate dielectric and stable V_{TH}. The outcomes of this project provide valuable information for developing desired GaN power devices with high performance, high stability and high reliability that meet the application standards.

1. Enhanced dynamic performance of GaN lateral heterojunction power FET

GaN power transistor with effectively suppressed current collapse has been realized by embedding a Schottky junction in the drain terminal of GaN HEMT device [13]. The on-chip photon pumping of electrons trapped in the deep levels can be achieved by the photons synchronously generated in the Schottky junction during hard-switch operation. Consequently, without epitaxy regrowth or over-designed buffer structures, the device dynamic performance can be significantly enhanced. The potentiality of on-chip hybrid opto-HEMTs to minimize the influences of deep traps during dynamic operation of AlGaN/GaN power HEMTs has been validated.

2. Interface treatment and interface protection for high quality interface with low D_{it}

Obtaining high-quality interface with low D_{it} is one of the most critical challenges in MIS-gate. According to a first-principles calculation study, the GaN surface states distribution can be modified by nitridation with the shallow trap (i.e. close to E_C) density greatly reduced [2]. Interface protection is another technique to prevent the GaN surface from degradation at high temperatures (~ 800 ^oC) [3] at which high-quality gate dielectric is deposited. The high temperature is necessary to obtain a densified dielectric film with reduced defect density.

3. High performance E-mode MIS-FET with high reliability and high stability

With the interface treatment and protection techniques, SiN_x gate dielectric (with the benefits of large conduction band offset of ~2.3 eV with GaN and relatively high dielectric constant of 7) deposited at 780 ^oC by LPCVD (low pressure chemical vapor deposition) is successfully integrated with recessed-gate structure to obtain E-mode MIS-FET [11]. With the reliable LPCVD-SiN_x gate dielectric and high quality interface, the high-performance MIS-FET delivers enhanced V_{TH} stability and gate dielectric reliability.

Reference

[1] S. Yang, C. Zhou, Q. Jiang, J. Lu, B. Huang, and K. J. Chen, "Investigation of buffer traps in AlGaN/GaN-on-Si devices by thermally stimulated current spectroscopy and back-gating measurement," *Appl. Phys. Lett.*, vol. 104, no. 1, p. 013504, Jan. 2014.

[2] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng, and K. J. Chen, "Impact of Substrate Bias Polarity on Buffer-Related Current Collapse in AlGaN/GaN-on-Si Power Devices," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5048–5056, Dec. 2017.

[3] S. Yang, S. Liu, Y. Lu, C. Liu, and K. J. Chen, "AC-Capacitance Techniques for Interface Trap Analysis in GaN-Based Buried-Channel MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1870–1878, Jun. 2015.

[4] S. Yang, S. Liu, C. Liu, Z. Tang, Y. Lu, and K. J. Chen, "Thermally induced threshold voltage instability of III-Nitride MIS-HEMTs and MOSC-HEMTs: Underlying mechanisms and optimization schemes," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, 2014, pp. 17.2.1-17.2.4.

[5] S. Yang, Y. Lu, H. Wang, S. Liu, C. Liu, and K. J. Chen, "Dynamic Gate Stress-Induced Shift and Its Impact on Dynamic in GaN MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 157–160, Feb. 2016.

[6] B. Li, X. Tang, and K. J. Chen, "Optical pumping of deep traps in AlGaN/GaN-on-Si HEMTs using an on-chip Schottky-on-heterojunction light-emitting diode," *Appl. Phys. Lett.*, vol. 106, no. 9, p. 093505, Mar. 2015.

[7] X. Tang *et al.*, "III-Nitride transistors with photonic-ohmic drain for enhanced dynamic performances," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 35.3.1-35.3.4.

[8] M. Hua *et al.*, "GaN-Based Metal-Insulator-Semiconductor High-Electron-Mobility Transistors Using Low-Pressure Chemical Vapor Deposition SiN_x as Gate Dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 448–450, May 2015.

[9] M. Hua *et al.*, "Characterization of Leakage and Reliability of SiN_x Gate Dielectric by Low-Pressure Chemical Vapor Deposition for GaN-based MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3215–3222, Oct. 2015.

[10] K. J. Chen *et al.*, "Surface nitridation for improved dielectric/III-nitride interfaces in GaN MIS-HEMTs," *Phys. Status Solidi A*, vol. 212, no. 5, pp. 1059–1065, May 2015.

[11] M. Hua *et al.*, "Integration of LPCVD-SiN_x gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 10.4.1-10.4.4.

Potential for further development of the research and the proposed course of action
(maximum half a page)

Based on the understanding of the bulk and interface traps in GaN-based power electronic devices, we have developed advanced device structures and process techniques to deliver the high-performance GaN MIS-HEMT/FET in this project. Toward the goal of widespread application of GaN power devices, the investigation of device reliability and stability will be our next topic. Presently, GaN power devices have entered the commercialization stage and have been used to demonstrate power conversion systems that have greater efficiency and higher power density than can be achieved with conventional Si power devices. However, a reliability qualification standards suitable for GaN-based devices, which recommend evaluation procedures to guarantee the qualified devices for safe and reliable application, is still not available. Because of the unique material and device physics of the GaN-based materials and devices, the testing methods and the lifetime prediction models recommended by the standards for Si CMOS are not sufficient for GaN power devices.

Therefore, a reliability evaluation and testing platform for commercial GaN power devices is desirable and should be developed in the future projects. At the center of this platform are novel power switching device characterization techniques, a fundamental understanding of reliability issues, credible lifetime predication models and systematic studies of challenging issues such as short-circuit capability and unclamped inductive switching capability. The future research topics will focus on the fundamental understanding of reliability issues and novel power device characterization methods. The reliability investigation will be conducted under various operating conditions of a power switch, which allows identification of the major reliability issues with different acceleration stress factors. Testing platforms will be set up to meet the requirements and support various stress conditions within a wide temperature range. These studies will provide the basic techniques and guidelines for device reliability evaluation and facilitate the establishment of reliability testing platform for GaN power devices.

7. The Layman's Summary

(describe in layman's language the nature, significance and value of the research project, in no more than 200 words)

Power semiconductors are at the heart of power conversion systems for electric energy processing. The continuous and recently accelerating electrification of modern society is demanding power semiconductor devices to deliver higher efficiency and higher power density. With superior material properties, wide-bandgap GaN power electronic devices are one of the most promising candidates for next-generation power converters that could significantly out-perform the Si-based devices. However, critical stability and reliability issues, most of which are caused by the bulk and interface traps have been hindering the commercialization of GaN power devices despite the strong interests from potential users. In this project, we conducted systematic and comprehensive investigation on the origins and underlying physical mechanisms of bulk and interface traps. Various techniques have been developed to study the diverse and dynamic behavior of bulk/interface traps and their effects on dynamic ON-state resistance and threshold voltage stability. Novel and effective solutions to the reliability issues have been invented and successfully developed, with results published and presented in prestigious journals and conferences.

Part C: Research Output

8. Peer-reviewed journal publication(s) arising directly from this research project

(Please attach a copy of each publication and/or the letter of acceptance if not yet submitted in the previous progress report(s). All listed publications must acknowledge RGC's funding support by quoting the specific grant reference.)

The Latest Status of Publications				Author(s) *(bold the authors belonging to the project teams and denote the corresponding author with an asterisk*)*	Title and Journal/Book *(with the volume, pages and other necessary publishing details specified)*	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*
Year of publication	Year of Acceptance	Under Review	Under Preparation *(optional)*					
2017				S. Yang*, C. Zhou, S. Han, J. Wei, K. Sheng, and **K. J. Chen**	"Impact of Substrate Bias Polarity on Buffer-Related Current Collapse in AlGaN/GaN-on-Si Power Devices," *IEEE Trans. Electron Devices,* vol. 64, no. 12, pp. 5048-5056, 2017.	31-12-2018	Yes	Yes
2017				S. Liu, M. Wang*, M. Tao, R. Yin, J. Gao, H. Sun, W. Lin, C. P. Wen, J. Wang, W. Wu, Y. Hao, Z. Zhang, **K. J. Chen**, **and B. Shen**	"Gate-Recessed Normally-OFF GaN MOSHEMT with Improved Channel Mobility and Dynamic Performance Using AlN/Si_3N_4 as Passivation and Post Gate-Recess Channel Protection Layers," IEEE Elec. Dev. Lett., vol. 38, No. 8, pp. 1075-1078, 2017.	31-12-2018	Yes	Yes
2017				Z. Zhang, B. Li, Q. Qian, X. Tang, M. Hua, B. Huang, and **K. J. Chen***	"Revealing the Nitridation Effects on GaN Surface by First-Principles Calculation and X-Ray/Ultraviolet Photoemission Spectroscopy," *IEEE Trans. Electron Devices*, vol. 64, No. 10, p. 4036-4036, 2017.	31-12-2018	Yes	Yes
2017				G. Tang, J. Wei, Z. Zhang, X. Tang, M. Hua, H. Wang, and **K. J. Chen***	"Dynamic R_{ON} of GaN-on-Si Lateral Power Devices with a Floating Substrate Termination," *IEEE Elec. Dev. Lett.*, vol. 38, No. 7, pp. 937-940, 2017.	31-12-2018	Yes	Yes
2016				B. Li, X. Tang, G. Tang, J. Wei, J. Wang, and **K. J. Chen***	"Switching Behaviors of On-Chip Photon Source on AlGaN/GaN-on-Si Power HEMTs Platform," *IEEE Photonics Technology Lett.*, vol. 28, pp. 2803-2806, 2016.	31-12-2018	Yes	Yes

2016				X. Tang, B. Li, Z. Zhang, G. Tang, J. Wei, and **K. J. Chen***	"Characterization of Static and Dynamic Behaviors in AlGaN/GaN-on-Si Power Transistors With Photonic-Ohmic Drain," *IEEE Trans. Electron Devices*, vol. 63, pp. 2831-2837, 2016.	31-12-2018	Yes	Yes
2016				J. Wei, H. Jiang, Q. Jiang, and **K. J. Chen***	"Proposal of a GaN/SiC Hybrid Field-Effect Transistor for Power Switching Applications," *IEEE Trans. Electron Devices*, vol. 63, pp. 2469-2473, 2016.	31-12-2018	Yes	Yes
2016				**K. J. Chen***, S. Yang, S. Liu, C. Liu, and M. Hua	"Toward reliable MIS- and MOS-gate structures for GaN lateral power devices," *Phys. Status Solidi A*, vol. 213, pp. 861-867, 2016.	31-12-2018	Yes	Yes
2016				B. Li, X. Tang, J. Wang, and **K. J. Chen***	"Optoelectronic Devices on AlGaN/GaN HEMT Platform," *Phys. Status Solidi A*, vol. 213, No. 5, pp. 1213-1221, 2016.	31-12-2018	Yes	Yes
2016				X. Tang, B. Li, Y. Lu, and **K. J. Chen***	"On-chip Addressable Schottky-on-Heterojunction Light-Emitting Diode Arrays on AlGaN/GaN-on-Si Platform, " *Phys. Status Solidi C*, vol. 13, No. 5-6, pp. 365–368, 2016.	31-12-2018	Yes	Yes
2016				S. Yang, Y. Lu, H. Wang, S. Liu, C. Liu, and **K. J. Chen***	"Dynamic Gate Stress-Induced V_{TH} Shift and Its Impact on Dynamic R_{ON} in GaN MIS-HEMTs," *IEEE Elec. Dev. Lett.*, vol. 37, pp. 157-160, 2016.	31-12-2018	Yes	Yes
2016				S. Yang, S. Liu, C. Liu, M. Hua, and **K. J. Chen***	"Gate stack engineering for GaN lateral power transistors," *Semicond. Sci. Technol.*, vol. 31, no. 2, p. 024001, 2016	31-12-2015	No	Yes
2015				S. Yang, S. Liu, Y. Lu, C. Liu, and **K. J. Chen***	"AC-Capacitance Techniques for Interface Trap Analysis in GaN-Based Buried-Channel MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1870–1878, Jun. 2015	31-12-2015	No	Yes

2015				S. Yang, Y. Lu, H. Wang, S. Liu, C. Liu, and **K. J. Chen***	"Dynamic Gate Stress-Induced V_{TH} Shift and Its Impact on Dynamic R_{ON} in GaN MIS-HEMTs," *IEEE Electron Device Lett.*, vol. PP, no. 99, pp. 1–1, 2015	31-12-2015	No	Yes
2015				J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and **K. J. Chen***	"Low On-Resistance Normally-Off GaN Double-Channel Metal-Oxide-Semiconductor High-Electron-Mobility Transistor," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015	31-12-2015	No	Yes
2015				Y. Lu, B. Li, X. Tang, Q. Jiang, S. Yang, Z. Tang, **K. J. Chen***	"Normally off Al_2O_3/AlGaN/GaN MIS-HEMT With Transparent Gate Electrode for Gate Degradation Investigation," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 821–827, Mar. 2015	31-12-2015	No	Yes
2015				C. Zhang, **M. Wang***, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, **K. J. Chen, and B. Shen**	"Temperature Dependence of the Surface- and Buffer-Induced Current Collapse in GaN High-Electron Mobility Transistors on Si Substrate," IEEE Transactions on Electron Devices, vol. 62, No. 8, pp. 2475-2480, Aug. 2015.	31-12-2015	No	Yes
2015				S. Lin, **M. Wang***, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, S. Huang, **K. J. Chen, and B. Shen**	"Reduction of Current Collapse in GaN High-Electron Mobility Transistors Using a Repeated Ozone Oxidation and Wet Surface Treatment," IEEE Electron Device Letters, vol. 36, No. 8, pp. 757-759, June 2015.	31-12-2015	No	Yes
2015				Y. Lu, Q. Jiang, Z. Tang, S. Yang, C. Liu, and **K. J. Chen***	"Characterization of SiN_x/AlN passivation stack with epitaxial AlN grown on AlGaN/GaN heterojunctions by plasma-enhanced atomic layer deposition," *Appl. Phys. Express*, vol. 8, no. 6, p. 064101, Jun. 2015	31-12-2015	No	Yes

2015				S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, **M. Wang, B. Shen**, and **K. J. Chen***	"Interface/border trap characterization of Al_2O_3/AlN/ GaN metal-oxide-semiconductor structures with an AlN interfacial layer," *Appl. Phys. Lett.*, vol. 106, no. 5, p. 051605, Feb. 2015	31-12-2015	No	Yes
2015				C. Liu, S. Yang, S. Liu, Z. Tang, H. Wang, Q. Jiang, and **K. J. Chen***	"Thermally Stable Enhancement- Mode GaN Metal-Isolator-Semiconductor High-Electron- Mobility Transistor With Partially Recessed Fluorine-Implanted Barrier," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 318–320, Apr. 2015	31-12-2015	No	Yes
2015				B. Li, X. Tang, and **K. J. Chen***	"Optical pumping of deep traps in AlGaN/GaN-on-Si HEMTs using an on-chip Schottky-on- heterojunction light-emitting diode," *Appl. Phys. Lett.*, vol. 106, no. 9, p. 093505, Mar. 2015	31-12-2015	No	Yes
2015				M. Hua, C. Liu, S. Yang, S. Liu, K. Fu, Z. Dong, Y. Cai, B. Zhang, and **K. J. Chen***	"GaN-Based Metal-Insulator-Semiconductor High-Electron- Mobility Transistors Using Low-Pressure Chemical Vapor Deposition SiN_x as Gate Dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 448–450, May 2015	31-12-2015	No	Yes
2015				M. Hua, C. Liu, S. Yang, S. Liu, K. Fu, Z. Dong, Y. Cai, B. Zhang, and **K. J. Chen***	"Characterization of Leakage and Reliability of SiN_x Gate Dielectric by Low-Pressure Chemical Vapor Deposition for GaN-based MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3215–3222, Oct. 2015	31-12-2015	No	Yes
2015				**K. J. Chen***, S. Yang, Z. Tang, S. Huang, Y. Lu, Q. Jiang, S. Liu, C. Liu, and B. Li	"Surface nitridation for improved dielectric/III-nitride interfaces in GaN MIS-HEMTs," *Phys. Status Solidi A*, vol. 212, no. 5, pp. 1059–1065, May 2015	31-12-2015	No	Yes

2014				S. Yang, S. Liu, C. Liu, Y. Lu, and **K. J. Chen***	"Mechanisms of thermally induced threshold voltage instability in GaN-based heterojunction transistors," *Appl. Phys. Lett.*, vol. 105, no. 22, p. 223508, Dec. 2014	31-12-2015	No	Yes
2014				S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, **M. J. Wang,** and **K. J. Chen***	"Al2O3/AlN/GaN MOS-Channel-HEMTs With an AlN Interfacial Layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 723–725, Jul. 2014	31-12-2015	No	Yes
2014				B. Li, X. Tang, J. Wang, and **K. J. Chen***	"P-doping-free III-nitride high electron mobility light-emitting diodes and transistors," *Appl. Phys. Lett.*, vol. 105, no. 3, p. 032105, Jul. 2014	31-12-2015	No	Yes

9. Recognized international conference(s) in which paper(s) related to this research project was/were delivered *(Please attach a copy of each delivered paper. All listed papers must acknowledge RGC's funding support by quoting the specific grant reference.)*

Month/Year/ Place	Title	Conference Name	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*
May/2017/Sapporo Japan	Buffer Trapping-Induced R_{ON} Degradation in GaN-on-Si Power Transistors: Role of Electron Injection from Si Substrate	*International Symposium on Power Semiconductor Devices IC's (ISPSD)*	31-12-2018	Yes	Yes
Dec/2016/ San Francisco USA	Nitridation of GaN Surface for Power Device Application: A First-Principles Study	*International Electron Devices Meeting (IEDM)*	31-12-2018	Yes	Yes
Dec/2016/ San Francisco USA	Integration of LPCVD-SiN_x Gate Dielectric with Recessed-gate E-mode GaN MIS-FETs: Toward High Performance, High Stability and Long TDDB Lifetime	*International Electron Devices Meeting (IEDM)*	31-12-2018	Yes	Yes
Jun/2016/Prague, Czech Republic	Impact of V_{TH} Shift on R_{ON} in E/D-Mode GaN-on-Si Power Transistors: Role of Dynamic Stress and Gate Overdrive	*International Symposium on Power Semiconductor Devices IC's (ISPSD)*	31-12-2018	Yes	Yes

Jun/2016/Prague, Czech Republic	Impact of Integrated Photonic-Ohmic Drain on Static and Dynamic Characteristics of GaN-on-Si Heterojunction Power Transistors	*International Symposium on Power Semiconductor Devices IC's (ISPSD*	31-12-2018	Yes	Yes
Dec./2015/Washington USA	III-nitride transistors with photonic-ohmic drain for enhanced dynamic performances	*International Electron Devices Meeting (IEDM)*	31-12-2015	No	Yes
May/2015/Hong Kong	Normally-off GaN MIS-HEMT with improved thermal stability in DC and dynamic performance	*International Symposium on Power Semiconductor Devices IC's (ISPSD)*	31-12-2015	No	Yes
May/2015/Hong Kong	650-V GaN-based MIS-HEMTs using LPCVD-SiNx as passivation and gate dielectric	*International Symposium on Power Semiconductor Devices IC's (ISPSD)*	31-12-2015	No	Yes
Dec./2014/ San Francisco USA	Thermally induced threshold voltage instability of III-Nitride MIS-HEMTs and MOSC-HEMTs: Underlying mechanisms and optimization schemes	*International Electron Devices Meeting (IEDM)*	31-12-2015	No	Yes
Dec./2014/ San Francisco USA	Schottky-on-heterojunction optoelectronic functional devices realized on AlGaN/GaN-on-Si platform	*International Electron Devices Meeting (IEDM)*	31-12-2015	No	Yes
Oct./2014/Guilin China	Nitridation interfacial-layer technology: Enabling low interface trap density and high stability in III-nitride MIS-HEMTs	*International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*	31-12-2015	No	Yes

10. Student(s) trained *(Please attach a copy of the title page of the thesis.)*

Name	Degree registered for	Date of registration	Date of thesis submission/ graduation
YANG, Shu	Ph.D	Sep.01 2010	Aug. 2014
JIANG, Qimeng	Ph.D.	Sep.01 2010	Dec. 2014
LU, Yunyou	Ph.D.	Sep.01 2010	Aug. 2015
TANG, Xi	Ph.D	Sep.01 2012	Aug. 2015
HUA, Mengyuan	Ph.D	Sep.01 2013	Aug. 2018

11. Other impact *(e.g. award of patents or prizes, collaboration with other research institutions, technology transfer, etc.)*