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The Research Grants Council of Hong Kong
NSFC/RGC Joint Research Scheme
Joint Completion Report

(Please attach a copy of the completion report submitted to the NSFC by the Mainland researcher)

Part A: The Project and Investigator(s)

1. Project Title

High Performance Resistive Phase Change Memory Technology for Terascale Storage
高性能相變存儲技術

2. Investigator(s) and Academic Department/Units Involved

	Hong Kong Team	Mainland Team
Name of Principal Investigator *(with title)*	Prof. Mansun CHAN (陳文新教授)	Prof. Zhitang Song (宋志棠教授)
Post	Professor (教授)	Professor (教授)
Unit / Department / Institution	Dept. of ECE/The Hong Kong University of Science & Technology (電子及計算機工程系/香港科技大學)	SIMIT/Chinese Academy of Science (上海微系统与信息技术研究所/中国科学院)
Contact Information	mchan@ust.hk	ztsong@mail.sim.ac.cn
Co-investigator(s) *(with title and institution)*		

3. Project Duration

	Original	Revised	Date of RGC/ Institution Approval *(must be quoted*)
Project Start date	January 1, 2013		
Project Completion date	Dec. 31, 2016		
Duration *(in month)*	48		
Deadline for Submission of Completion Report	Dec. 31, 2017		

Part B: The Completion Report

5. Project Objectives

5.1 Objectives as per original application

1. Study critical phase-change conditions of phase-change material with different geometry under different operation conditions based on atomic level simulation
2. Perform thermal analysis that and with the result from atomic level simulation to understand the phase change action at different operation modes.
3. Implement a compact model based on the study in this work for circuit simulation. The model will include the results from the material study, thermal cross-talk between neighboring devices and device reliability under prolonged operation.
4. Based on the result of the theoretical study in (1)-(3), experimentally investigate the design of PCM cells including both the phase change material and driving devices to achieve

reduced programming power and increased memory density. Both traditional and new designs will be used for the purpose of demonstration as well as validation of the model developed in this project. This part of the work will be performed together with the Chinese partner.

5. Together with the Chinese partners, demonstrate a high-density cross-point memory array compatible with mainstream logic technology

5.2 Revised Objectives

Date of approval from the RGC: N/A

Reasons for the change: _____

_____

6. Research Outcome

Major findings and research outcome
(maximum 1 page; please make reference to Part C where necessary)

Following the project objectives, we have transferred the atomistic ab-initio simulator developed by our collaborator, Prof. Hong Guo's group at McGill University to our own computer platform and further enhance its functionality to incorporate disorder theory and atomic movements during the phase change material programming. It allowed us to study the detail crystallization in a phase change material during SET and RESET. The results have been reported in 2014 EDSSC (Conf. [2][3][4]). Using the detail results from the atomic simulation, we are able to predict both the size of the active region and the degree of crystallization. Before this work, all PCM model assumed a constant active region volume independent of the

temperature and time. This is the first time the size of the active region of the active volume is included in a circuit model. The calculation of the active volume has been reported in Conf. [5]. Combining with a conformal mapping method to transform the 3D spread resistance into a simple parallel electrode geometry, we have obtained a simple expression for the SET and RESET resistance. The 3D resistance has been implemented into a complete model and was reported in Journal [1] together with earlier capacitance calculation we developed (Conf. [1]) for delay prediction.

For a functional model, accuracy is only one of the criteria. Coverage, convergence, functional smoothness, implementability are equally important to make the model usable beyond publication. The latter part, however, are hardwork that may not result in larger number of publication. We managed to have the model implemented in Verilog-A code and passed all the tests with experimental data provided by our partners in mainland. Now, the model code has been made available to other researchers through the NEEDS (Nano-Engineered Electronic Device Simulation Node) platform of the Nanohub (https://nanohub.org/groups/needs) and implemented in the interactive Modeling and Online Simulation (i-MOS) platform (http://i-mos.org). It represents our commitment to produce a functional model for the research community beyond pure publications.

Based on the models we developed, we have studied ways to solve the high programming power problem in PCM memory. We have identified the solution of concentrating the thermal energy over a very small area corresponding to the active region to be the most effective approach. There are two approaches to achieve, namely increasing the interface resistance and reducing the contact area between the bottom electrode and the phase change material. Both methods have been studied and the model predictions have been reported in Conf. [7][8]. We have further developed a technique to achieve the minimum possible cross-section area of the bottom electrode using carbon nanotube for the bottom contact. The idea has been experimentally verified and published in Conf. [6] and Journal [2].

We have developed all the components for a cross-point memory system. As the ultimate goal of the project, we hope to demonstrate a prototype of a functional cross-point memory array together with the timing and read/write circuits. This would require a stable production level process and logistic support. However, the development of PCM technology in our partner SMICS is only in preliminary state and all the design rules, technology files and standard cell library are not yet ready. To manage the situation, we have decided to separate the memory technology and system design. And we would like to demonstrate the novelty we achieved in system level architecture. To do this, we have to use a more mature memory cell to replace the function of the PCM cell in our targeted application. And we have decided to apply the designs to the cache memory in CPU using SRAM as the memory element instead of a PCM material. The approach is to demonstrate in system level that the proposed architecture is fully functional. When production level PCM cells are ready from any foundry, they can be used to replace the SRAM to form a complete system. The resulting circuits with SRAM cell are published in Journal [3][4] due to the novelty of the circuit architecture alone. And both papers have acknowledged that the designs were solely support by this project.

Potential for further development of the research and the proposed course of action
(maximum half a page)

In this project, we have developed all necessary components to design and fabricate a resistive based memory system based on phase-change memory technology. Unfortunately, the availability of production technology is not under our control. Through the collaboration between our group and our mainland partner, we have established a process to quickly incorporate experimental results generated in mainland to a complete circuit model developed by our group that eventually engineers in the two group to optimize the device structure as well as doing system design. This has

significantly shortened the time to transfer device level progress to applications. With this framework, we believe that system level prototype can be design quickly once the production level PCM memory cell technology is made available to us. Application design as system level such as neuromorphic computing should be pursued once the technology become mature.

7. The Layman's Summary

(describe in layman's language the nature, significance and value of the research project, in no more than 200 words)

With the current computing technology entering the age of "big-data", real time analytics and processing of enormous quantities of data is necessary. However, the performance gap between the processor and the memory has been growing, which has become the most significant limitation in data processing. In addition, the grow of neuromorphic computing requires a different mersister type of memory instead of traditional capacitive based flash memory. To meet the challenges, phase-change memory (PCRAM) is the most promising technology as it is the most mature technology relatively to other new resistive based memory.

Even though PCM technology is more mature and promising than other resistive memory based technology, there are still a number of problems to resolve, with the most critical ones being: (1) lack of understanding on the material properties that correspond to various output characteristics; (2) high current required to perform RESET with unoptimized structures; (3) lack of a detailed model for predicting interaction between the PCM cell and the driving circuits; (4) a methodology for studying reliability issues including thermal cross-talk and data retention. In this project, we have addressed the problems described above to provide a foundation for future phase change memory system development.

Part C: Research Output

8. Peer-reviewed journal publication(s) arising directly from this research project

(Please attach a copy of each publication and/or the letter of acceptance if not yet submitted in the previous progress report(s). All listed publications must acknowledge RGC's funding support by quoting the specific grant reference.)

The Latest Status of Publications				Author(s) ***(bold** the authors belonging to the project teams and denote the corresponding author with an asterisk*)*	Title and Journal/ Book *(with the volume, pages and other necessary publishing details specified)*	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
Year of publication	Year of Acceptance *(For paper accepted but not yet published)*	Under Review	Under Preparation *(optional)*						
2014				**Yihan Chen*,** K. C. Kwong**, Xinnan Lin, Zhitang Song, and Mansun Chan**	3-D Resistance Model for Phase-Changel Memory Cell, IEEE Transactions on Electron Devices, vol. 61, no. 12, December 2014	Yes (2015)	No	Yes	No
2017				**Panni Wang*, Yihan Chen, Suwen Li, Salahuddin Raju, Longyan Wang, Lining Zhang, Xinnan Lin, Zhitang Song and Mansun Chan**	Low Power Phase Change Memory with Vertical Carbon Nanotube Electrode, IEEE Journal of the Electron Device Society, vol. 5, Issue 5, September 2017, pp. 362-366	No	Yes	Yes	No

2017				**Khawar Sarfraz* and Mansun Chan**	A 1.2V-to-0.4V 3.2GHz-to-14.3MHz Power-Efficient 3-Port Register File in 65-nm CMOS, IEEE Transactions on Circuits and Systems I, vol. 64, no. 2, February 2017, pp. 360-372	No	Yes	Yes	No
2017				**Khawar Sarfraz* and Mansun Chan**	A 140-mV Variation-Tolerant Deep Sub-Threshold SRAM in 65-nm CMOS, IEEE Journal of Solid-State Circuit, vol. 52, issue 8, Aug. 2017, pp. 2215-2220	No	Yes	Yes	No

9. Recognized international conference(s) in which paper(s) related to this research project was/were delivered *(Please attach a copy of each delivered paper. All listed papers must acknowledge RGC's funding support by quoting the specific grant reference.)*

Month/Year/ Place	Title	Conference Name	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
June/2014/ Chengdu, China	Critical Parasitic Capacitance in Nano-scale Phase-change Memory (PCM) Cell	2014 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2014)	Yes	No	Yes	No
June/2014/ Chengdu, China	Atomistic Simulation of Phase Change Memory During Switching	2014 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2014)	Yes	No	Yes	No
June/2014/ Chengdu, China	Study on Nucleation Characteristic of Phase Change Memory Set Operation Using Numerical Simulation	2014 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2014)	Yes	No	Yes	No
June/2014/ Chengdu, China	Transition from Junction Limited to Bulk Limited Subthreshold Conduction in Phase Change Memory	2014 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2014)	Yes	No	Yes	No
April/2015/ Taiwan	Modeling Active Dimension for Phase Change Memory Cell	2015 VLSI-TSA	No	Yes	Yes	No
April/2015/ San Francisco, USA	All-Carbon Interconnect: Integration Strategy and Implication for Memory Applications	2015 MRS Spring Meeting and Exhibit	No	Yes	Yes	No

June/2016/ Singapore	Interface Engineering to Enhance Phase Change Memory Programmability	2015 IEEE Conference on Electron Devices and Solid-State Circuits	No	Yes	Yes	No
August/2016 /Hong Kong	Modeling Current Reduction for PCM Cell with Thermal Buffer Layer	2016 IEEE International Conference on Electron Device and Solid-State Circuits	No	Yes	Yes	No

10. Student(s) trained *(Please attach a copy of the title page of the thesis.)*

Name	Degree registered for	Date of registration	Date of thesis submission/ graduation
Yihan Chen	PhD	September 2012	August 2016
Khawar Sarfrax	PhD	September 2012	August 2016
Suwen Li	PhD	September 2014	August 2017
Panny Wang	MPhil	September 2015	June 2017

11. Other impact *(e.g. award of patents or prizes, collaboration with other research institutions, technology transfer, etc.)*

We have developed a fully functional compact model for phase change memory with more advanced feature than the existing one and the source codes in Verilog-A has been released through the NEEDS platform of Nanohub (https://nanohub.org/groups/needs) and implemented in the interactive Modeling and Online Simulation (i-MOS) platform (http://i-mos.org).