RGC Ref.: N_HKU715/14 NSFC Ref. : 51461165301
(please insert ref. above)

The Research Grants Council of Hong Kong
NSFC/RGC Joint Research Scheme
Joint Completion Report

(Please attach a copy of the completion report submitted to the NSFC by the Mainland researcher)

Part A: The Project and Investigator(s)

1. Project Title

Organic memory array fabricated under ambient air environment: from polycrystalline thin film to single crystal devices

2. Investigator(s) and Academic Department/Units Involved

	Hong Kong Team	Mainland Team
Name of Principal Investigator *(with title)*	Paddy Kwok Leung CHAN, Dr.	Hanying Li, Prof.
Post	Associate Professor	Professor
Unit / Department / Institution	Mechanical Engineering, The University of Hong Kong	Department of Polymer Science & Engineering, Zhejiang University
Contact Information	pklc@hku.hk	hanying_li@zju.edu.cn
Co-investigator(s) *(with title and institution)*		

3. Project Duration

	Original	Revised	Date of RGC/ Institution Approval *(must be quoted*)
Project Start date	01/01/2015		
Project Completion date	31/12/2018		
Duration *(in month)*	48		
Deadline for Submission of Completion Report	31/12/2019		

Part B: The Completion Report

5. Project Objectives

5.1 Objectives as per original application

5.2 Under ambient air environment, use large area screen-printing and ink-jet printing methods to deposit the gate, source and drain electrodes on the memory transistor on flexible substrates;

2. Develop an universal ultrasonic spray coating system to co-deposit organic semiconductor and metal nanoparticles under ambient air environment;

3. Investigate the flow speed, flow pattern, concentration ratio of semiconductor/metal blend and the effects of solvents on the size and distribution of the embedded nanoparticles and thus the memory window of the thin film memory transistors;

4. Employ droplet-pinned crystallization method to integrate nanoparticles into the single crystal organic memory transistors;

5. Integrate 16×16 individual memory transistors in series to form the NAND structure memory and demonstrate their application potentials on unconventional substrate for practical application.

5.3 Revised Objectives

N. A.

6. Research Outcome

Major findings and research outcome

Solution processing technique for large area memory transistor active layer

We have invented two ambient environment solution processing techniques, known as dual solution shearing (Adv. Funct. Mat., 27, 1700999, 2017) and nucleation seed-controlled shearing (ACS Appl. Mater. and Inter., 2018), to deposit organic semiconductor active layers. The dual solution shearing technique allows us to develop monolayer or bilayer organic crystal with excellent uniformity. The nucleation seed-controlled solution shearing allows us to produce large area organic single crystal up to inch scale. Based on these two methods, we can generate a highly uniform organic single crystal for the photolithography process. It is an important step to scale down the dimensions of the memory transistor. It also provides an opportunity to increase the device density for the more sophisticated circuits. Recently, we demonstrated the first transistor array based on the monolayer C_{10}-DNTT single crystal developed by direct photolithography processing (Adv. Mat., submitted, 2019).

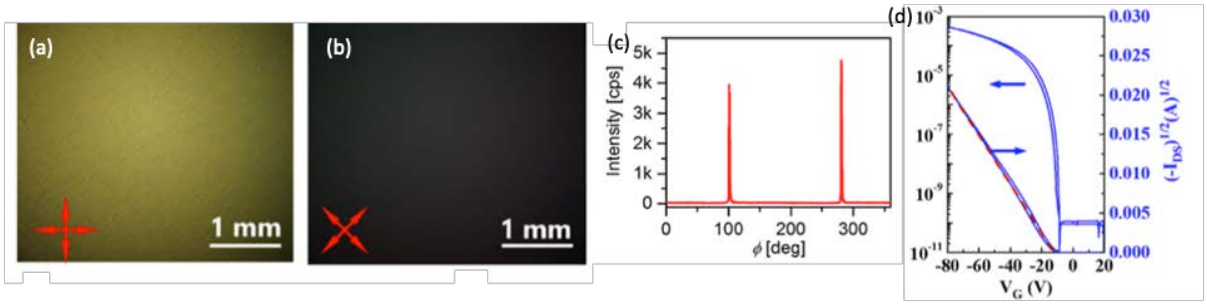

Figure 1(a) and (b) Polarized light microscopy images of the large area organic crystal without grain boundaries. (c) grazing incident in-plane phi-scan of the organic semiconductor active layers. The two peaks are exactly 180°

different which suggests the film is a high quality single crystal. (d) The typical transfer curves of the grain boundary-free organic transistor.

Memory transistor array

We have combined screen printing, spray coating, evaporation, and solution shearing to develop an active matrix organic memory transistor array in the NAND structure (Adv. Mat. , 30, 1706647, 2018). In the structure, we have carefully designed the shared bit-lines, word-lines and the gate-lines among the 16□16 array structure. Since these electrodes are shared among different devices, the failure of one line would cause the malfunction of the whole array circuit which requires highly reliable fabrication techniques. The yield rate of our processing recipe is higher than 95%, and all the testing and characterizations are controlled by a LabVIEW program. The charge retention time achieved by our device is longer than 20000s.

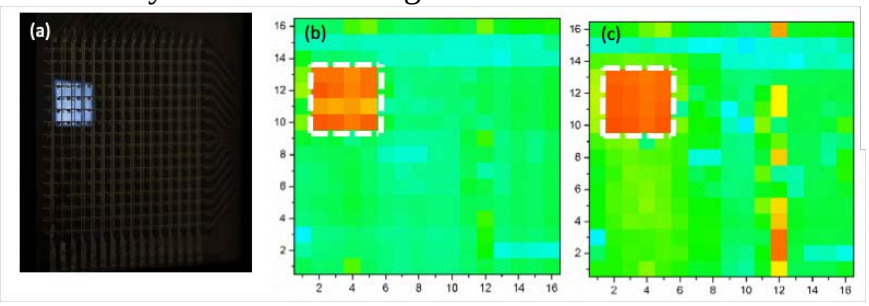

Figure 2 (a) The optical image of the memory array program under white light illumination. The current reading of the memory array (n) right after and (c) 2 hours after the programming process.

Better understanding on the physical limit of the memory transistor devices

In this project, we pay a particular focus on understanding the actual physical limitations of the memory transistors such as the contact resistance issue, problems induced by downsizing, and the mobility overestimation. All these challenges must need to be addressed in order to make the advantages of organic memory transistors available. Based on that, we spend a particular focus on studying the drawbacks of (i) decreasing the device size (Adv. Elec. Mat., submitted 2019) and the (ii) mobility overestimation in the memory transistor (ACS Appl. Elect. Mat., submitted, 2019)

Potential for further development of the research and the proposed course of action *(maximum half a page)*

The results obtained in this project have brought positive impacts to the development of organic memory transistors. It makes the organic semiconductor single crystal suitable for the direct patterning by photo- or e-beam lithography. This allows the organic semiconductors to have the side-by-side comparison with the traditional inorganic semiconductors. The significant advantage of the organic-based memory device is their flexibility and low fabrication cost. While keeping these advantages, the functionality of the device should not be degraded. To maintain the functionality, the number of data storage element has to be comparable with the inorganic counterparts. It would inevitably require decreasing the dimensions of the memory transistors. When the channel length and electrode contact area are decreased, the ratio between the contact resistance to the channel resistance will increase, and in the extreme cases, the contact resistance may dominate the whole device. As a result, the next step development of the memory transistor should focus on improving the contact resistance problem in organic memory transistors. Possible directions include but not limited to (i) doping effect at the organic metal interface, (ii) new structures to enhance charge injection, (iii) ultrathin active layer to enhance charge injection from the

electrodes to the channel. All these directions are the physics-rich area which worth for further investigations by the researchers in this field.

7. The Layman's Summary

(describe <u>in layman's language</u> the nature, significance and value of the research project, in no more than 200 words)

Information storage is an essential element in the modern electronic devices. Traditionally, these information storage devices are based on the circuit chips developed on silicon. Although the storage capacity of these inorganic devices are still dominating, their compatibility with the next generation flexible electronics and circuits has become a great concern. Different from the conventional silicon, the flexible electronics use organic semiconductor as the active layers are holding together by van der Waals force so that it can have extremely high flexibility and ductility. Devices like foldable display and wearable photovoltaics have been successfully demonstrated. Unconventional substrates such as fiber based paper, banknotes, human skin and etc are suitable for these new devices. However, in order to make these organic electronic devices have comparable functions and performances with silicon devices, the development of flexible memory transistor on plastic substrates would be a critical step. In this current project, we have successfully developed new structure of memory transistors based on organic crystals and flexible substrates. The performance of our devices is good enough for the memory buffer applications. These devices have great application potentials to integrate with other components in the flexible circuit to achieve a truly flexible organic circuit.

<u>Part C: Research Output</u>

8. Peer-reviewed journal publication(s) arising <u>directly</u> from this research project

(Please attach a copy of each publication and/or the letter of acceptance if not yet submitted in the previous progress report(s). All listed publications must acknowledge RGC's funding support by quoting the specific grant reference.)

The Latest Status of Publications				Author(s) *(**bold** the authors belonging to the project teams and denote the corresponding author with an asterisk*)*	Title and Journal/ Book *(with the volume, pages and other necessary publishing details specified)*	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
Year of publication	Year of Acceptance *(For paper accepted but not yet published)*	Under Review	Under Preparation *(optional)*						

		2019		**B. Peng, X. Ji,** M. Chu, J. Liu, Y. Li, M. Chen, Z. Zhou, C. Zhang, Q. Miao, H. Dong, B. Huang, W. Hu, S. P. Feng, W. Li and **P. K. L. Chan***,	Overcoming the substrate limitations: an active layer transfer method for high-performance flexible electronics	No	No	Yes	Yes
		2019		**K. Pei, M. Chen, Z. Zhou, H. Li, P. K. L. Chan***	Overestimation of Carrier Mobility in Organic Thin Film Transistors Due to Unaccounted Fringe Currents	No	No	Yes	Yes
2018	2018			**Z. W. Zhou, Z. C. Zhang**, Q. S. Wu, X. D. Ji, J. L. Wang , X. C. Zeng , S.-P. Feng and **P. K. L. Chan***	Inch-Scale Grain Boundary Free Organic Crystals Developed by Nucleation Seed-Controlled Shearing Method	No	Yes	Yes	Yes
2018	2018			**X. D. Ji,** P. C. Zhou, L. Zhong, A. M. Xu, A. C. O. Tsang and **P. K. L. Chan***	Smart Surgical Catheter Integrated with Imperceptible Organic Transistor for C-Reactive Protein Sensing	No	Yes	Yes	Yes

2018	2017			**K. Pei, X. C. Ren, Z. C. Zhang, X. D. Ji, P. K. L. Chan***	A High-Performance Optical Memory Array Based on Inhomogeneity of Organic Semiconductors	No	Yes	Yes	Yes
2017	2017			**Z. C. Zhang, B. Y. Peng, X. D. Ji, K. Pei and P. K. L. Chan***	Marangoni Effect-Assisted Bar Coating Method for High Quality Organic Crystals with Compressive and Tensile Strains	No	Yes	Yes	Yes
2017	2017			**S. Y. Huang, B. Y. Peng and P. K. L. Chan**	Ambipolar Organic Field-effect Transistors based on Dual-functional, Ultra-thin and Highly Crystallized 2,9-didecyldinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene (C10-DNTT) Layer	No	Yes	Yes	Yes

2016	2016			**Z. Huang, G. Xue, J. Wu, S. Liu, H. Li,** Y. Yang, F. Yan, **P. K. L. Chan**, H. Chen and **H. Li***	Electron transport in solution-grown TIPS-pentacene single crystals: effects of gate dielectrics and polar impurities	Yes	No	Yes	Yes
2016	2016			**B. Y. Peng**, Z. R. Wang and **P. K. L. Chan***	A simulation-assisted solution-processing method for a large-area, high-performance C10-DNTT organic semiconductor crystal	2017	No	Yes	Yes
2016	2016			K. W. Cheuk, **K. Pei** and **P. K. L. Chan***	Degradation mechanism of a junction-free transparent silver network electrode	2017	No	Yes	Yes
2016	2016			X. C. Ren, **K. Pei**, **B. Y. Peng**, Z. C. Zhang, Z. R. Wang, X. Y. Wang, and **P. K. L. Chan***	Low operating power and flexible active matrix organic transistor temperature sensors array	2017	No	Yes	Yes

9. Recognized international conference(s) in which paper(s) related to this research project was/were delivered *(Please attach a copy of each delivered paper. All listed papers must acknowledge RGC's funding support by quoting the specific grant reference.)*

Month/Year/ Place	Title	Conference Name	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
August, 2018, San Diego	High-performance field effect transistors based on multiple solution processing and the stain effects in the organic crystals	SPIE Organic Photonics + Electronics	No	Yes	Yes	Yes
April, 2018,Guangzhou	Organic field effect transistors array for optical memory applications	International Conference of Display Technology, Society for Information Display (SID)	No	Yes	Yes	Yes
December, 2016, Boston	Flexible Nonvolatile Optical Memory Transistors utilizing Intrinsic Charge Trapping in an Organic Semiconductor	Materials Research Society Fall meeting	Yes	No	Yes	Yes
December, 2015, Boston	Anodized Oxide Network Dielectric Based on Crack Template Masking and Its Application in Low Driving Voltage Organic Transistors	Materials Research Society Fall meeting	Yes	No	Yes	Yes

10. Student(s) trained *(Please attach a copy of the title page of the thesis.)*

Name	Degree registered for	Date of registration	Date of thesis submission/

			graduation
Ke Pei	PhD degree	1/4/2015	1/10/2019

11. Other impact *(e.g. award of patents or prizes, collaboration with other research institutions, technology transfer, etc.)*

One application patent is currently under consideration by the technology transfer office of HKU.