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(please insert ref. above)

The Research Grants Council of Hong Kong
NSFC/RGC Joint Research Scheme
Joint Completion Report

(Please attach a copy of the completion report submitted to the NSFC by the Mainland researcher)

Part A: The Project and Investigator(s)

1. Project Title

Cross-layer Analysis and Optimization for the Lifetime Reliability of MPSoCs

2. Investigator(s) and Academic Department/Units Involved

	Hong Kong Team	Mainland Team
Name of Principal Investigator *(with title)*	Dr. Xu, Qiang	Dr. Yang, Huazhong
Post	Associate Professor	Professor
Unit / Department / Institution	Computer Science & Engineering / The Chinese University of Hong Kong	Electrical Engineering / Tsinghua University
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Co-investigator(s) *(with title and institution)*	Dr. Cao, Yu Associate Professor Computer Science & Engineering / Arizona State University	Dr. Xie, Yuan Professor Computer Science & Engineering / Pennsylvania State University Dr. Wang, Yu Associate Professor Electronic Engineering / Tsinghua University

3. Project Duration

	Original	Revised	Date of RGC/ Institution Approval *(must be quoted*)
Project Start date	2013-01-01	N.A.	N.A.

Project Completion date	2016-12-31	N.A.	N.A.
Duration *(in month)*	48	N.A.	N.A.
Deadline for Submission of Completion Report	2017-12-31	N.A.	N.A.

Part B: The Completion Report

5. Project Objectives

5.1 Objectives as per original application

1. To develop a full-system lifetime reliability simulation framework for MPSoCs
2. To investigate novel cross-layer optimization techniques to meet the lifetime reliability requirement of MPSoCs;
3. To optimize dynamic reliability management policy online to achieve better system performance and/or energy-efficiency without violating lifetime reliability constraint;

5.2 Revised Objectives

Date of approval from the RGC: N.A.

Reasons for the change: _____

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1.
2.
3. ....

6. Research Outcome

Major findings and research outcome
(maximum 1 page; please make reference to Part C where necessary)

In our DAC'14 paper, we developed an accurate yet efficient simulation framework for NBTI-induced performance degradation, which is a major lifetime reliability threat for integrated circuits. To be specific, we first presented a comprehensive NBTI analytical model that explicitly takes supply voltage, duty cycle and temperature variations into consideration. The accuracy of the proposed model is validated against cycle-accurate simulation for NBTI effects. In addition, based on the proposed model, we present a novel simulation framework for system lifetime prediction by running representative workloads only. Experimental results demonstrate that the proposed solution is much more accurate than previous solutions.

In our ITC'15 paper, we investigate the impact of clock-TSV aging in three-dimensional integrated circuits and the countermeasures to mitigate it. To be specific, we propose to insert aging sensors in the circuit and put a tunable buffer following each clock-TSV. The runtime information of the triggered alarms in these aging sensors are used for efficient and effective online diagnosis, with which we further propose three online diagnosis and clock tuning methods to diagnose the root cause of the failure, associated with an efficient tuning algorithm for each method. Experimental results show that dramatic reliability enhancement is achieved with the proposed solutions.

Timing error is a serious concern for the lifetime reliability of integrated circuits. In our ICCAD'13 paper, we proposed a new forward timing error correction scheme, namely ForTER, which predicts whether the occurrence of timing errors would propagate to the next level of sequential elements and corrects them without necessarily borrowing timing slack. The proposed technique can be combined with other timing error resilient circuit design techniques to further improve circuit performance, as demonstrated in our experimental results with various benchmark circuits.

A large and growing number of applications are inherently error-tolerant, which do not require "strict" correctness but rather approximate correctness. We have proposed several approximate computing techniques (ICCAD'13, GVLSI'15, ICCAD'15) to tradeoff reliability and performance to achieve better energy-efficiency, including approximate adder design, approximate memory access, and approximate techniques for large-scale Eigen decomposition.

Security flaws in integrated circuits prevent the normal operation of integrated circuits during their lifetime. In this project, we have also investigated several security issues (ICCAD'14, ASPDAC'15, ICCAD'15), including probing attack, Trojan side-channel, and physical unclonable functions.

Potential for further development of the research and the proposed course of action *(maximum half a page)*

Approximate computing has gained significant tractions in recent years, but it is still in its infancy. We are extending the proposed research to tackle the various problems in approximate computing. To be specific, we plan to monitor application quality variations at runtime and conduct dynamic quality management to achieve controlled quality-efficiency tradeoffs in approximate computing.

7. The Layman's Summary

(describe in layman's language the nature, significance and value of the research project, in no more than 200 words)

By considering the inherent correlations between failure mechanisms and the impact of runtime workloads, we develop novel hierarchical analytical model and cross-layer simulation and optimization framework for the lifetime reliability of integrated circuits. As system failures during the warrantee period not only incur high replacement cost but also damage the reputation of the system provider, the significance and value of the project is evident.

Part C: Research Output

8. Peer-reviewed journal publication(s) arising directly from this research project

(Please attach a copy of each publication and/or the letter of acceptance if not yet submitted in the previous progress report(s). All listed publications must acknowledge RGC's funding support by quoting the specific grant reference.)

The Latest Status of Publications				Author(s) ***(bold** the authors belonging to the project teams and denote the corresponding author with an asterisk*)*	Title and Journal/ Book *(with the volume, pages and other necessary publishing details specified)*	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
Year of publication	Year of Acceptance *(For paper accepted but not yet published)*	Under Review	Under Preparation *(optional)*						

9. Recognized international conference(s) in which paper(s) related to this research project was/were delivered

(Please attach a copy of each delivered paper. All listed papers must acknowledge RGC's funding support by quoting the specific grant reference.)

Month/Year/ Place	Title	Conference Name	Submitted to RGC *(indicate the year ending of the relevant progress report)*	Attached to this report *(Yes or No)*	Acknowledged the support of this Joint Research Scheme *(Yes or No)*	Accessible from the institutional repository *(Yes or No)*
11/2013/ San Jose	ForTER: a forward error correction scheme for timing error resilience	International Conference on Computer-Aided Design	2014	Yes	Yes	Yes
11/2013/ San Jose	On reconfiguration-oriented approximate adder design and its application	International Conference on Computer-Aided Design	2014	Yes	Yes	Yes

06/2014/ San Francisco	On the Simulation of NBTI-Induced Performance Degradation Considering Arbitrary Temperature and Voltage Variations	Design Automation Conference	2014	Yes	Yes	Yes
11/2014/ San Jose	On Trojan side channel design and identification	International Conference on Computer-Aided Design		Yes	Yes	Yes
01/2015/ Chiba, Japan	Vulnerability analysis for crypto devices against probing attack	Asia Pacific Design Automation Conference		Yes	Yes	Yes
05/2015/ Pittsburgh	ApproxMA: Approximate Memory Access for Dynamic Precision Scaling	ACM Great Lakes Symposium on VLSI		Yes	Yes	Yes
10/2015/ Anaheim	On diagnosable and tunable 3D clock network design for lifetime reliability enhancement	International Test Conference		Yes	Yes	Yes
11/2015/ Austin	ApproxEigen: An Approximate Computing Technique for Large-Scale Eigen-Decomposition	International Conference on Computer-Aided Design		Yes	Yes	Yes
11/2015/ Austin	BoardPUF: Physical Unclonable Functions for Printed Circuit Board Authentication	International Conference on Computer-Aided Design		Yes	Yes	Yes

10. Student(s) trained *(Please attach a copy of the title page of the thesis.)*

Name	Degree registered for	Date of registration	Date of thesis submission/ graduation
Wang, Ting	Ph.D.	08/2012	03/2017
Zhang, Qian	Ph.D.	08/2013	08/2017

Tian, Ye	Ph.D.	08/2015	08/2019 Approximate Accelerator Design and Optimization

11. Other impact *(e.g. award of patents or prizes, collaboration with other research institutions, technology transfer, etc.)*

N.A.