GERMANY/HONG KONG JOINT RESEARCH SCHEME
THE PROJECT REPORT
(for Project Completion)

Project Number: 9053009 (G_HK010/10)

Title

Lightweight Formal Methods for Power and Timing Analysis of Memory Architectures

Particulars

	Hong Kong team	German team
Name of Project Co-ordinator (with title)	Dr. Chun Jason Xue	Prof. Samarjit CHAKRABORTY
Name of Co-Investigator (if any)		Dr. Benedikt DIETRICH
Institution or Institutional affiliation	x CityU; HKU; CUHK; HKUST; HKBU; LU; HKIEd; PolyU	University of _____; Others: Technische Universitat Munchen
Other project team members (if any)		

Funding Period

	1st year	2nd year (if applicable)
Start Date	01-Jan-2011	01-Jan-2012
Completion Date	31-Dec-2011	31-Dec-2012

Objective(s) as per original application

1. Develop models, analysis techniques and algorithms to systematically analyze the influence of different memory architectures on application performance (in particular timing properties) and power consumption.
2. Investigate cache locking techniques to improve the timing predictability of safety-critical applications.
3. Develop design and analysis techniques for modern memory technologies like flash and other non-volatile memories (like Phase Change Memory and Magnetic RAMs), with the goal of improving the longevity of such memories, improving timing predictability and reducing power consumption.
4. Implement the developed analysis and design methods into prototype tools.

Details of Report [Please attach relevant document(s)]

i) Outline of proposed research and results obtained

The following are the results so far from this project:

- We identify that when multiple control applications running on an ECU, the order of execution has a significant impact on the cache re-use analysis which leads to different WCET. As a result, we propose a technique to optimize control performance based on careful ordering of control applications based on WCET with cache re-use analysis.
- For ECUs with cache locking capability, when multiple control applications runs, we identify that current approach of cache locking to minimize total WCET is not the optimal for control performance. Hence, we propose a technique to optimize control performance with cache locking and partitioning for multi-tasking environment.

ii) Significance of research results

The results from this project have significant impact on control application optimization. With the same amount of hardware and the same architecture, the proposed techniques can achieve better control performance for free.

iii) Research output

Currently several papers are under progress.

iv) Potential for or impact on further research collaboration

Based on discussions and progress we have made during this project, we identify that there is a significant space that we can target to explore software and architecture optimization for control performance. We wish to continue the collaboration after the completion of the project.